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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/048,933	03/26/1998	DEAN A. KLEIN	MEI-97-01386	4879

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EXAMINER
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TRAN, TRANG U

ART UNIT	PAPER NUMBER
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2622

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/048,933

Applicant(s)

KLEIN, DEAN A.

Examiner

Trang U. Tran

Art Unit

2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 06 February 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 and 12-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 12-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>02/06/2006</u> . | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on February 06, 2006 has been entered.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3, 5-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al (US Patent No. 5,812,789) in view of Melo et al (US Patent No. 6,040,845).

In considering claim 1, Diaz et al discloses all the claimed subject matter, note 1) the claimed receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system

Art Unit: 2622

bus is met by the decoder/encoder 45 which is integrated into a core logic chipset 150 and coupled to a processor (Central Processing Unit or CPU) 152, peripherals such as a hard disk drive 164 and a Digital Versatile Disk (DVD) CD-ROM 166, a bus such as a PCI bus 170 and the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4), 2) the claimed computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein, the difference frame including computing the difference frame in the core logic chip within the computer system is met by the decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62), 3) the claimed storing the difference frame in directly from the core logic chip to the system memory in the computer system via a dedicated memory interface therebetween is met by the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56), and 4) the claimed the processor retrieving the difference frame directly from the system memory via the core logic chip using a dedicated processor interface therebetween to complete compression of the video data is met by a processor (Central Processing Unit or CPU) 152 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56).

However, Owen et al explicitly do not disclose the claimed wherein the core logic

chip is a north bridge chip.

Melo et al teach that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target (Fig. 1, col. 1, line 47 to col. 2, line 32 and col. 4, lines 18-65).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention to incorporate accelerator (core logic unit) with the teaching of graphic accelerator that is provided either at the North bridge chip for the stated advantage as taught by Melo et al into Diaz et al's system in order to achieve MIPS (millions of instructions per second) without substantially loading the PCI (peripheral component interface).

In considering claim 2, the claimed including storing the current video frame in the system memory in the computer system is met by the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56 of Diaz et al).

In considering claim 3, the claimed wherein the current video frame is written over a previous video frame in the system memory is met by the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56 of Diaz et al).

In considering claim 5, the claimed wherein computing the difference frame includes computing a difference between a block of data from the current video frame and a block of data from the previous video frame is met by the decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and

access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62 of Diaz et al).

In considering claim 6, the claimed wherein storing the difference frame in memory includes storing the difference frame in the system memory using block transfers is met by the main memory 168 which couple to the memory interface 48 through the memory bus 167 (Fig. 3, col. 8, line 30 to col. 9, line 4 of Diaz et al).

In considering claim 7, the claimed including compressing the video data using the difference frame to produce compressed video is met by the decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62 of Diaz et al).

In considering claim 8, the claimed including performing a color space conversion on the video data is met by the graphics accelerator (with video scaler and color space converter) 188 (Fig. 3, col. 8, line 30 to col. 9, line 4 of Diaz et al).

In considering claim 9, the system of Diaz et al and Melo et al discloses the claimed invention as discussed in claim 1 above, except for providing the claimed including using the video data in compressed form in a video teleconferencing system. Since examiner takes Official Notices that it is notoriously well-known in the art for the usage of the compressed video data form in a teleconference system, whereof the compressed video data format transmission provides the benefit of bandwidth

conservation on the communication linking medium. Therefore it is submitted that it would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Diaz et al and Melo et al accordingly in order to facilitated the video teleconferencing and to make efficient use of the bandwidth on the communication link.

In considering claim 12, the claimed wherein computing the difference frame includes computing the difference frame in circuitry outside of a central processing unit in the computer system is met by the decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62 of Diaz et al).

4. Claims 4 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al (US Patent No. 5,812,789) in view of Melo et al (US Patent No. 6,040,845), and further in view of Abramatic et al (US Patent No. 4,546,383).

In considering claim 4, the combination of Diaz et al and Melo et al disclose all the limitations of the instant invention as discussed in claim 1 above, except for providing the claimed wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame. Abramatic et al. teaches that a form of image compression consists the detecting variations (difference) between one image and the next one as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the

current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention to incorporate XOR function for the difference calculation as taught by Abramatic et al into the combination of Diaz et al and Melo et al' system in order to providing a less complicated means for the difference calculation techniques as elucidate at column 7, lines 32-35 of Abramatic et al.

In considering claim 13, Owen et al discloses all the claimed subject matter, note 1) the claimed receiving a current video frame at a dedicated video input of a core logic chip in the computer system directly from a video source originating the video frame, the computer system including the core logic chip for directly coupling a processor to a system memory and for coupling the processor and the system memory to a system bus is met by the decoder/encoder 45 which is integrated into a core logic chipset 150 and coupled to a processor (Central Processing Unit or CPU) 152, peripherals such as a hard disk drive 164 and a Digital Versatile Disk (DVD) CD-ROM 166, a bus such as a PCI bus 170 and the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4), 2) the claimed computing at the core logic chip a difference frame from the current video frame and a previous video frame as the current video frame streams into the dedicated video input of the core logic chip, the previous video frame being received at the core logic chip as a previous current video frame and retained therein is met by the



Art Unit: 2622

decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62), 3) the claimed storing the difference frame in directly from the core logic chip into the system memory in the computer system via a dedicated memory interface therebetween is met by the main memory 168 which is couple to the memory interface 48 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56), 4) the claimed storing the current video frame in directly from the core logic chip into the system memory in the computer system using a dedicated processor interface therebetween is met by a processor interface 154 of the core logic device (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56), 5) the claimed the processor retrieving the difference frame directly from the system memory via the core logic chip is met by a processor (Central Processing Unit or CPU) 152 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56), and 6) the claimed compressing the video data using the difference frame to produce compressed video data is met by a processor (Central Processing Unit or CPU) 152 and the encoder/decoder 45 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56).

However, Diaz et al explicitly do not disclose: 1) the claimed wherein the core logic chip is a north bridge chip, and 2) the claimed the difference frame including computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference

frame in the core logic chip within the computer system.

1) Melo et al teach that using conventional master/slave nomenclature, the graphics accelerator can be considered an AGP compliant master, the north bridge, and specifically, the memory controller or core logic within the north bridge can be partially considered as an AGP compliant target (Fig. 1, col. 1, line 47 to col. 2, line 32 and col. 4, lines 18-65). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention to incorporate accelerator (core logic unit) with the teaching of graphic accelerator that is provided either at the North bridge chip for the stated advantage as taught by Melo et al into Diaz et al's system in order to achieve MIPS (millions of instructions per second) without substantially loading the PCI (peripheral component interface).

2) Abramatic et al. teaches that a form of image compression consists the detecting variations (difference) between one image and the next one as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention to incorporate XOR function for the difference calculation as taught by Abramatic et al into the combination of Diaz and Melo et al' system in order to providing a less complicated means for the difference calculation techniques as

elucidate at column 7, lines 32-35 of Abramatic et al.

In considering claim 14, the claimed wherein the current video frame is written over a previous video frame in the system memory is met by the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56 of Diaz et al).

In considering claim 15, the claimed wherein computing the difference frame includes computing a difference between a block of data from the current video frame and a block of data from the previous video frame is met by the decoder/encoder 45 which are capable of both intrapicture compression and interpicture compression, and access to the previous or future image that contains information needed to decode or encode the current image and only the different information is transferred for interpicture compression (Fig. 2, col. 7, line 5 to col. 8, line 62 of Diaz et al).

In considering claim 16, the claimed wherein storing the difference frame in system memory includes storing the difference frame in the system memory using block transfers is met by the main memory 168 which couple to the memory interface 48 through the memory bus 167 (Fig. 3, col. 8, line 30 to col. 9, line 4 of Diaz et al).

In considering claim 17, the system of Diaz et al, Melo et al and Abramatic et al discloses the claimed invention as discussed in claim 13 above, except for providing the claimed including using the video data in compressed form in a video teleconferencing system. Since examiner takes Official Notices that it is notoriously well-known in the art for the usage of the compressed video data form in a teleconference system, whereof the compressed video data format transmission provides the benefit of bandwidth conservation on the communication linking medium. Therefore it is submitted that it

Art Unit: 2622

would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the system of Diaz et al, Melo et al and Abramatic et al accordingly in order to facilitated the video conferencing and to make efficient use of the bandwidth on the communication link.

In considering claim 18, the claimed including performing a color space conversion on the video data is met by the graphics accelerator (with video scaler and color space converter) 188 (Fig. 3, col. 8, line 30 to col. 9, line 4 of Diaz et al).

In considering claim 19, the claimed including storing instructions and data for the computer system in the system memory is met by the main memory 168 (Fig. 3, col. 8, line 30 to col. 9, line 4 and col. 11, lines 28-56 of Diaz et al).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (571) 272-7358. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT  
May 15, 2006



Trang U. Tran  
Examiner  
Art Unit 2622